**Open Review**

( ) I would not like to sign my review report  
(x) I would like to sign my review report

Quality of English Language

(x) I am not qualified to assess the quality of English in this paper  
( ) English very difficult to understand/incomprehensible  
( ) Extensive editing of English language required  
( ) Moderate editing of English language required  
( ) Minor editing of English language required  
( ) English language fine. No issues detected

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|  | Yes | Can be improved | Must be improved | Not applicable |
| Does the introduction provide sufficient background and include all relevant references? | ( ) | (x) | ( ) | ( ) |
| Are all the cited references relevant to the research? | ( ) | (x) | ( ) | ( ) |
| Is the research design appropriate? | ( ) | (x) | ( ) | ( ) |
| Are the methods adequately described? | ( ) | ( ) | (x) | ( ) |
| Are the results clearly presented? | ( ) | ( ) | (x) | ( ) |
| Are the conclusions supported by the results? | ( ) | (x) | ( ) | ( ) |

Comments and Suggestions for Authors

Q1.Is the FinFET modeled through simulation calibrated with measured data? The calibration of a device generated by simulation is necessary to prove this research is meaningful using simulation.

Q2. Is each insulator material's interface trap considered at the Si-Insulator interface?

Q3. It is hard to analyze the graph in this study. Need the resolution of the figure.

Q4. In the single dielectric condition, on-current is enhanced as the dielectric constant increases. It is a fact that results are in the ideal case. Meanwhile, if High-K materials are deposited on the silicon channel, the interface trap is further generated at the Si-High K interface than at the Si-SiO2 interface. Also, carrier mobility at the Si-gate dielectric interface is degraded. On-current will be degraded above phenomenon. Could you demonstrate the on-current tendency in the un-ideal case (interface trap generated) compared with the ideal case (non-interface trap condition)?

Q5. Need the detailed gate dielectric tunneling mechanism. Please improve the electron tunneling mechanism beyond the gate dielectric.

Q6. The gate dielectric tunneling mechanism is analyzed using the equivalent dielectric constant when the electrons tunnel beyond the gate dielectric. Please explain the tendency of the gate current in the gate dielectric stacking case, such as SiO2- Al2O3-HfO2, which does not use an equivalent dielectric constant.

Q7. For referring to gate dielectric tunneling, did you use the quantum model? A quantum model should be applied to describe the exact gate tunneling mechanism in the thin dielectric material (< 2 nm). I think the hot carrier injection probability of the electrons fluctuates when the quantum model is used in the gate dielectric stacking case, not the equivalent dielectric constant. Please compare the gate dielectric stacking, such as SiO2- Al2O3-HfO2 without equivalent dielectric constants, with the equivalent dielectric method applying the quantum model.

Submission Date

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